REMARKS

Claims 1 - 28 remain in the application, in which claims 21, 23 - 28 are allowed. Claims 1, 2, 12, 14 - 16, 18, 20 and 22 have been amended. Applicants respectfully request for allowance of each of pending claims 1 - 28.

Claims 12 and 14- 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in an independent form including all of the limitations of the base claim and any intervening claims. Claims 12, 14 - 16 and 18 have been rewritten as independent claims including all of the limitations of their base claims and intervening claims. Thus, these claims are now in a condition of allowance. Accordingly, claims 13, 17 and 19 dependent thereupon are also now in a condition of allowance.

The Rejections under 35 U.S.C. §102

Claims 1 - 2 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,008,970 to Maloney et al. (hereinafter referred to as "Maloney").

The amended independent claim 1 is directed to an electrostatic discharge (ESD) protection circuit having an objective to dissipate an electrostatic pulse. The circuit comprises an ESD pulse clamp means comprising a PMOS device for shunting the electrostatic pulse from an integrated circuit (IC). A voltage inverter directly controlling a gate electrode of the PMOS device functions as a part of an ESD detection means that detects a presence of the electrostatic pulse. The inverter assures that the ESD pulse clamp means will not be turned on during the normal operation of the IC.

Maloney describes a much complicated circuit design, as can be seen in FIG. 2. Although Maloney also teaches an ESD protection mechanism, the design of such mechanism is quite different from the claimed invention. Maloney proposes a PMOS transistor 202 controlled by a control circuit 204 adapted to pull the gate of the PMOS transistor 202 below ground during an ESD event to increase current sinking (see FIG. 2 and col. 3 lines 31 - 37). A capacitor 212 operates as a pump capacitor which forces the gate of the PMOS transistor 202 to a negative voltage (see FIG. 2 and col. 3 line 66 - col. 4 line 1). As such, there is no teaching of using an inverter to control the gate of a PMOS transistor directly.

Since claims 2 and 10 dependent on the amended independent claim 1 they are not anticipated by Maloney.

The Rejections under 35 U.S.C. §103

Claims 3 - 9, 11, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ker (IEEE Transactions on Electron Devices Vol.46 No.1) in view of Maloney.

As discussed above with regard to the rejection of claim 1, Maloney does not by itself teach the claimed invention. Claims 3 - 9 and 11 depend on the amended claim 1, and, therefore, are also patentable. Putting aside the reasons illustrated above, for discussion purposes here, Ker and Maloney still should not form the basis for rejecting these claims.

As it is known, the Examiner bears the initial burden to establish a prim facie case of obviousness. When evaluating a claim for determining obviousness, all

limitations of the claim must be evaluated, and the invention must be examined as a whole. If the Examiner does not produce a prima facie case, Applicants are under no obligation to submit evidence of non-obviousness.

Ker teaches an NMOS device operating as an ESD pulse clamp (see FIG. 7). As discussed in Applicants' correspondence dated on May 19, 2003, it is difficult to couple a high voltage to the substrate of an NMOS device, while a high voltage is readily coupled to the N-well of a PMOS device. Thus, the difference between Ker's NMOS device and the PMOS device of the claimed invention is significant. Nowhere in Ker suggests that its NMOS device may be replaced with a PMOS device. Furthermore, there is no suggestion in Maloney to use an inverter for controlling the gate of the PMOS device directly. There is no sufficient showing that it would haven been obvious to combine Ker with Maloney. Therefore, it is believed that the rejection under 35 U.S.C. 103 relied on Ker and Maloney is inappropriate.

As such, the dependent claims 3 – 9 and 11, and the amended independent claim 20 are patentable over the cited art as well.

CONCLUSION

Applicants have made an earnest attempt to place this application in an allowable form. In view of the foregoing remarks, it is respectfully submitted that the pending claims are drawn to novel subject matter, patentably distinguishable over the prior art of record. The Examiner is therefore, respectfully requested to reconsider and withdraw the outstanding rejections.

Should the Examiner deem that any further clarification is desirable, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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